M.S. THESIS

Characterization of Trap Generated By Process and Cycling Stress in 26 nm NAND Flash Memory

26 나노 NAND Flash Memory에서 공정과정과 스트레스로 인해서 생성된 트랩의 분석

BY

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이 논문을 공학석사 학위논문으로 제출함

2013 년 2 월

서울대학교 대학원

전기컴퓨터공학부

조 봉 수

조봉수의 공학석사 학위논문을 인준함

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ABSTRACT

Trap in 26 nm NAND flash memory was characterized in terms of bit-line (BL) current fluctuation (ΔI_{BL}), extraction of trap position in 3-D space (x_T, y_T, and z_T) of the tunneling oxide and trap energy (E_t). Especially, percolation path could be identified and accurate z_T could be obtained, using the states of adjacent cells. Then, ΔI_{BL}, S_I/I_{BL}^2, capture (τ_c) and emission times (τ_e) of RTN were measured before and after cycling stress, respectively. With cycling stress, S_I/I_{BL}^2 and ΔI_{BL} were increased significantly. τ_c and τ_e of RTN after cycling stress are shorter by about 2~3 times than those of RTN generated by process stress. With the program (P) and erase (E) states of adjacent cells, ΔI_{BL} and corner frequency (f_c) of Lorentzian spectrum are changed. Using measured ΔI_{BL} and extracted τ_c and τ_e with 4 different modes (P/P, P/E, E/P, E/E), we calculated τ and f_c, and extracted the position of a trap in the channel width direction with ΔI_{BL} and simulated data. The calculated data showed excellent agreement with measured spectra. Finally, trap was characterized with the

method charge pumping method.

Key Words : RTN, Cycling Stress, NAND Flash, Trap, Capture and Emission Time, Charge Pumping.

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CONTENTS

1. Introduction

Recently, NAND flash memory has been widely used as a mass data storage device and the size of data has increased. In order to meet ever increasing market demand of storage capacity, aggressive efforts for scaling NAND flash devices have been made. As an example, the cell size in planar channel NAND flash memory has been scaled down to 15 nm node [1]. As the result of the scaling-down, NAND flash memory has been faced with various problems such as read disturbance, cell-to-cell interference, program saturation issue, and so on [2]-[3]. Among these problems, RTN which is caused by the capture/emission of an electron at a trap inside tunneling oxide becomes one of the critical issues, because increasing ΔI_{BL} with scaling-down of cell size can make an error during read operation and the memory unreliable[4]. Especially, the trap which is responsible for RTN can be not only generated during fabrication process but also generated by cycling stress. Though, lots of works have been published

regarding significant increase of RTN amplitude [5], the difference between process and stress induced traps are not clarified yet with respect to their temporal parameters and their spatial positions. In a previous paper [6], a methodology to extract the 3-D position of trap generated by process was introduced. Moreover, we suggest new method to extract more accurate z_T by considering percolation path. In this work, we investigate systematically RTN generated by process and cycling stress induced traps.

In Chapter 2, we introduce the method to extract 3-D position of trap. The methodology introduced in [6]. Then, we propose the methodology to extract more accurate z_T with the effect of percolation path.

In Chapter 3, we characterize RTN generated by process and cycling stress induced Traps in 26 nm NAND flash memory. To check RTN generated by cycling stress induced trap, first, we measured I_{BL} in time domain and normalized noise power spectral density (S_I/I_{BL}^2). Here, I_{BL} is 100 nA when bit-line voltage (V_{BL}) and pass voltage (V_{PASS}) are 0.8 and 6.5, respectively. Then we measured I_{BL} and S_I/I_{BL}^2 at the same bias condition after 1 k and 2 k cycling.

2. Extraction of 3-D Position of Trap in 26nm NAND Flash Memory

In this work, we characterized NAND flash cell strings fabricated with 26 nm technology. It consists of sixty-four cells, two dummy cells, a drain select line (DSL) transistor and a source select line (SSL) transistor. The channel length and width are 26 nm and 20 nm, respectively. The block diagram of the RTN measurement system was represented in Fig. 1.

To observe ΔI_{BL}, the biases were applied to flash cells by using dc power supply (SR 570 low-noise current preamplifier) and semiconductor parameter analyzer (Agilent 4155C), respectively. ΔI_{BL} was amplified by the low-noise current preamplifier and was displayed on the dynamic signal analyzer (Agilent 35670A).

Then, we study the position of traps responsible for RTN in x-y plane, because the effect of traps is quite different with the position of traps. We extracted the position of traps (x_T: a trap position within the tunneling oxide from the channel

surface, y_T: a trap position within tunneling oxide along the channel length direction from the left edge of the control gate) by using the method in a literature [6]. In extracting the position of traps, channel resistance effect except that of a read cell should be considered because a cell string consists of sixty-four unit cells, two dummy cells, and two select transistors (a DSL and a SSL). The measured devices have a tunneling oxide thickness of 7.9 nm. Fig. 2 shows the extracted x_T and y_T for process induced traps in 30 cells. We understand the traps are roughly located around both edges of the channel, which seems to be come from the gate etch process [7].

In order to extract a trap position along the channel width direction (z_T), we also use the method in the literature [6]. In Fig. 3, the change of simulated ΔI_{BL} with the z_T as a parameter of the state (program or erase) of adjacent BL cells was shown when the x_T in the tunneling oxide is 1 Å. The bias condition used in this simulation is exactly the same as above (I_{BL} = 100 nA, V_{BL} = 0.8 V and V_{PASS} =6.5 V). Simulated ΔI_{BL}s are shown along the channel width direction with the state of adjacent BL cells. For example, if ΔI_{BL} is 70 nA, the high level

current is 100 nA and the low level current is 30 nA. P/P mode means that adjacent cells are both programmed (V_{th} = 3 V). The V_{th} of a read cell is set to 0 V. In E/E mode, both adjacent BL cells are erased (V_{th} = -3 V). Based on the behavior of ΔI_{BL} with the state of adjacent BL cells, we can extract the position of z_T.

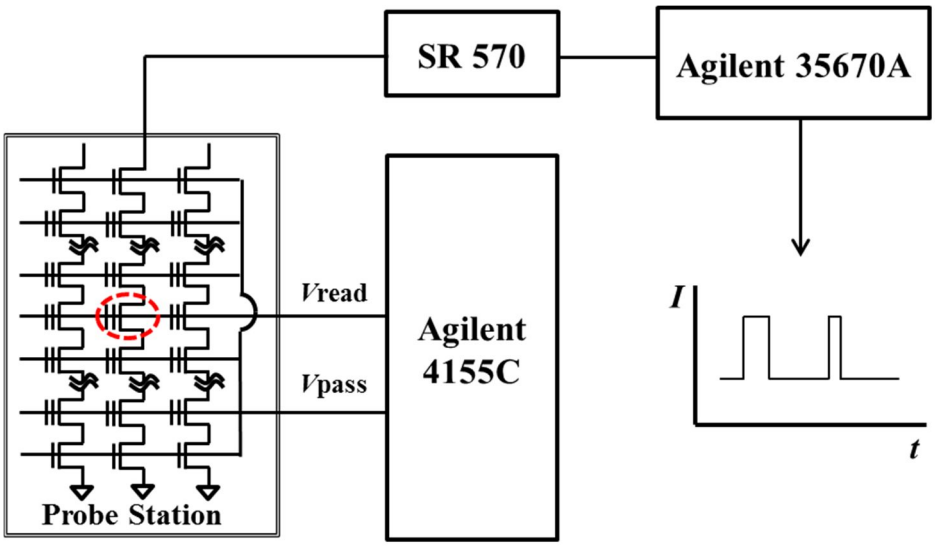

Fig. 1. Block diagram of RTN measurement system. SR 570 serves as dc power supply and low-noise current amplifier, Agilent 4155C functions to supply biases (signal and ground), and Agilent 35670A serves to display noise data in time domain.

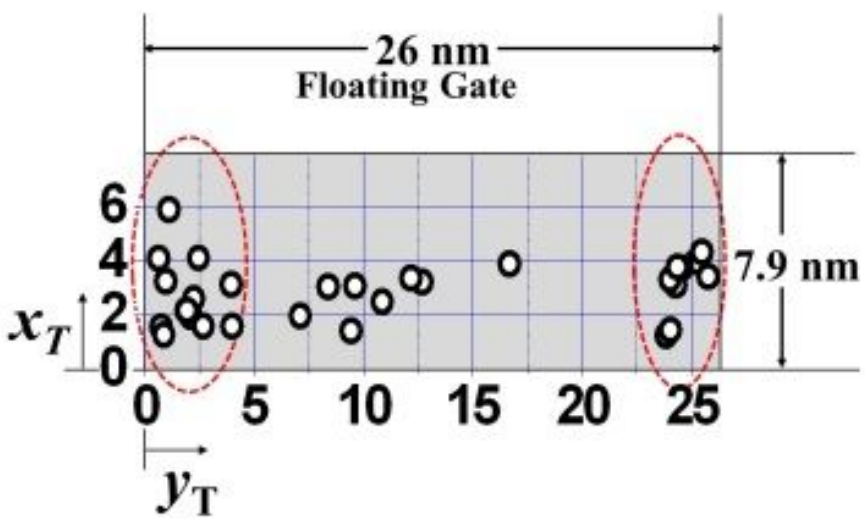

Fig. 2. Extracted vertical (x_T) and lateral (y_T) trap positions of process induced traps in the tunneling oxide

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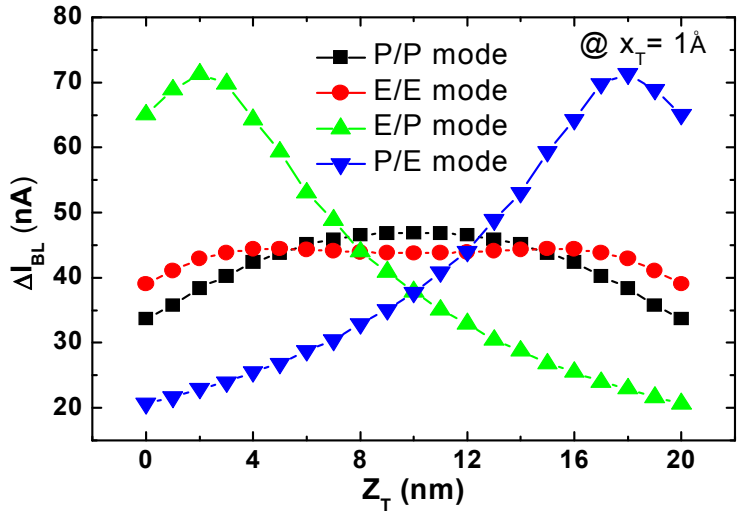


Fig. 3. Simulated ΔI_{BL} with a trap position along the channel width (z_T) as a parameter of the state (program or erase) of adjacent BL cells when the trap depth (x_T) is 1 Å.

3. The effect of adjacent cells and extraction of more accurate position of z_T with percolation path

To extract z_T, we measure ΔI_{BL} of a cell in a mode among P/P, E/E, E/P, and P/E modes of adjacent cells in adjacent BLs. For example, P/P means both adjacent cells are programmed. Fig. 4 shows the measured ΔI_{BL} of a read cell with 4 different modes (P/P, E/E, E/P and P/E modes) of the state of adjacent cells in a 26 nm NAND flash memory string in time domain. I_{BL} was fixed at 100 nA when the V_{BL} is 0.8V and a V_{pass} of 6.5 V is applied to pass cells. The adjacent cell is programmed to have a V_{th} of 3 V or erased to have a V_{th} of -3 V and the read cell is set to have a V_{th} of 0 V. Then, we extracted ΔI_{BL}, τ_c and τ_e. Fig. 5 shows RTN amplitude distribution with 4 different modes of adjacent BL cells. The inset represents a part of measured RTN waveform where the low I_{BL} is changed with the state of adjacent cells as shown in Fig.4. Here, low and high I_{BL}s represent the decreased and increased I_{BL}s, respectively, due to the capture

and emission of an electron at a trap. In this example, ΔI_{BL} due to RTN ranges from ~67.3 nA to ~45.9 nA with 4 different modes of the state of adjacent cells. Based on the transconductance of the cell with different modes, we can obtain V_{th}s corresponding to ΔI_{BL}s. The range of the ΔV_{th} is about 0.13 V ~ 0.18 V depending on the modes. From the result in Fig.5, ΔI_{BL} increases by about 46.6% when the mode of adjacent cells is changed from P/E mode to P/P mode. Using measured ΔI_{BL} and extracted τ_c , τ_e and g_m with 4 modes in Figs. 4 and 5, we can calculate τ, f_c and ΔV_{th} using equations in Table.1.[8] Fig 6 shows normalized power spectral density of a cell in a cell string with 4 different modes of adjacent cells. Red dotted lines represent modeled data from the equation in Table. 1. Fig.7 shows the change of simulated ΔI_{BL} with a trap position along z_T as a parameter of the state of adjacent BL cells when x_T in the tunneling oxide from the channel surface is 1 Å. A method to extract x_T and z_T was explained in our previous work. The ΔI_{BL}s are obtained at I_{BL} of 100 nA. Bias condition in Fig. 7 is exactly the same as that in Figs. 4 and 5. If ΔI_{BL} is 70 nA, the high level current is 100 nA and the low level current is 30 nA. Based on the behavior of

ΔI_{BL} with the state of adjacent BL cell, we can extract the position of z_T. The position of z_T is at 7.8 nm from the left edge of the channel width. Considering a total channel width of 20 nm, the trap is located at slightly left side from the center of the channel. However, the amplitude of ΔI_{BL}s with different modes is different from that of simulated ΔI_{BL}s. Therefore we can assume the existence of percolation path nearby the trap position and further research about the effect of percolation path is required. To see the effect of adjacent BL cells, we prepared energy band diagrams in P/P and P/E modes which were obtained by 3-D device simulation at I_{BL} = 100 nA. In Fig. 8, the band bending in P/P mode is steeper than the one in P/E mode, because the gate bias in P/P mode needs to be higher than that in P/E mode to keep the same I_{BL} of 100 nA (read current).

The z_T of ~60% of traps could be extracted by using the method in [6] in which percolation path is controlled by the state of adjacent BL cells. To extract z_T of remaining ~40% of traps, we introduced a percolation path caused by process variation. Fig. 9 shows 3-D simulated electron current density in y-z plane without a percolation path (a) and with a percolation path at 10 nm in z-

direction (b). Here, the percolation width is 2 nm. Since E/P mode is assumed, the current density near z_T of 0 nm is the largest as shown in Fig. 9 (a). But the current densities at z_T of 0 nm and the percolation path in Fig. 9 (b) are comparable. Fig. 10 shows extracted trap position in y-z plane of the tunneling oxide. In Fig. 10 (a), crossed square symbols have an error in only z position, because those positions cannot be explained by the fingerprint shown in Fig. 11 (a). In this case, we can use new fingerprint obtained by considering percolation path shown in Fig. 11 (b) where the percolation path is located at 2 nm, 6 nm, and 10 nm (the center of body width). As an example, we corrected two positions represented by curved arrow marks shown in Fig. 11 (a). Fig. 11 (b) compares accurate z_T position of traps induced by process (solid squares) and cycling stress (open circles) in y-z plane. In both figures, traps are located generally in the edge region in y-direction and located in the region except both edges in z-direction.

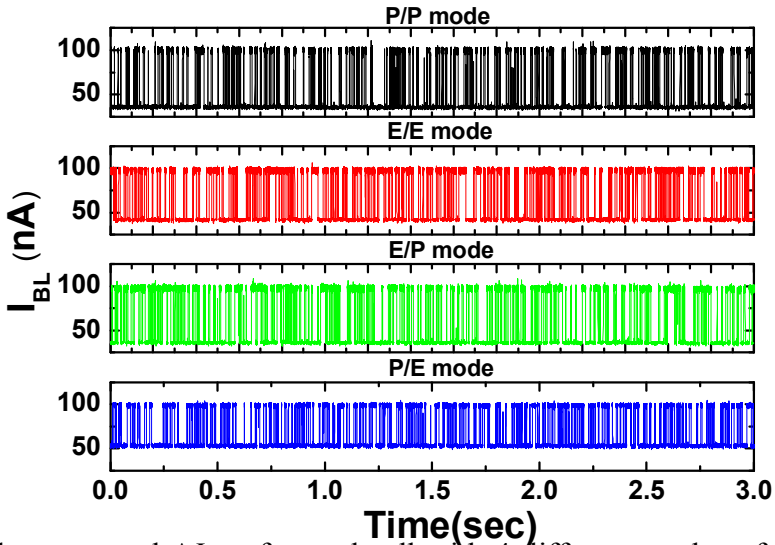


Fig. 4. The measured ΔI_{BL} of a read cell with 4 different modes of the state of adjacent cells in a 26 nm NAND flash memory strings. I_{BL} is fixed at 100 nA when V_{BL} and V_{pass} are 0.8 and 6.5 V, respectively. The adjacent cell is programmed to have a V_{th} of 3 V or erased to have a V_{th} of -3 V and the read cell is set to have a V_{th} of 0 V.

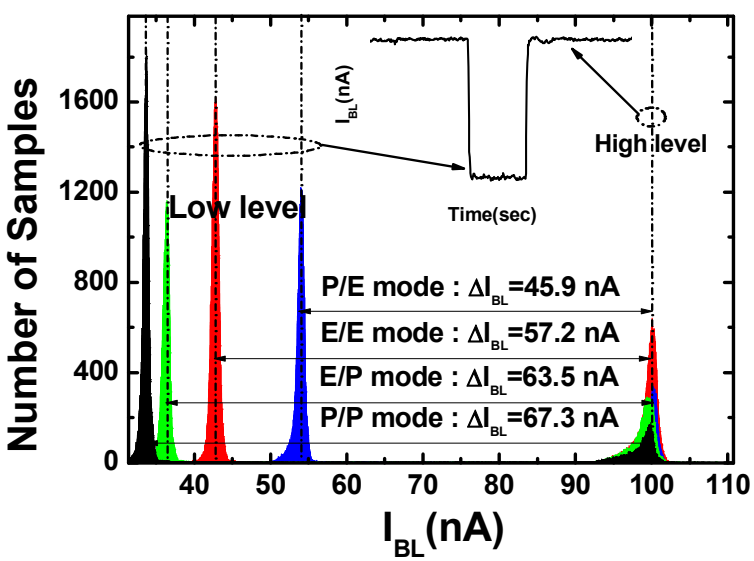


Fig. 5. RTN amplitude distribution with 4 different modes of adjacent BL cells. Measured ΔI_{BL} changes depending on the cell state of adjacent cells. (P/P, E/E, E/P, and P/E modes).

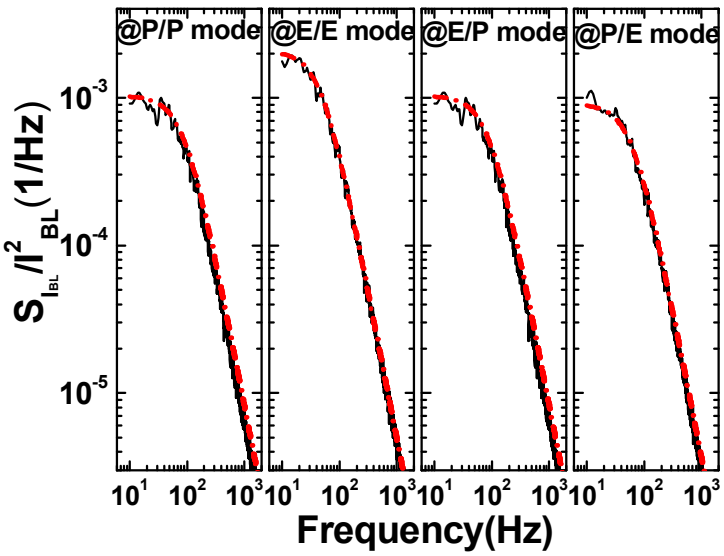


Fig. 6. Normalized power spectral density of a cell in a cell string with 4 different modes of adjacent cells. Red dash-dot lines represent modeled data

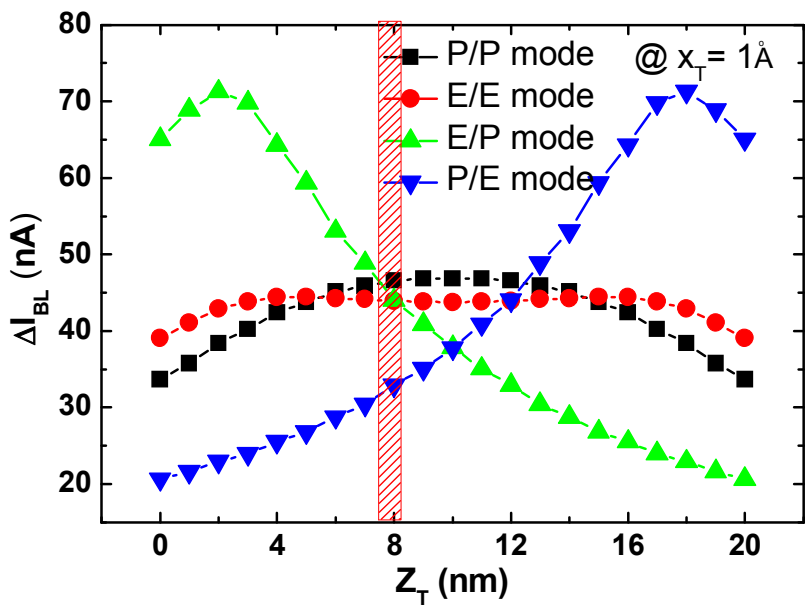


Fig. 7. Simulated ΔI_{BL} with a trap position along z_T as a parameter of the state of adjacent BL cells

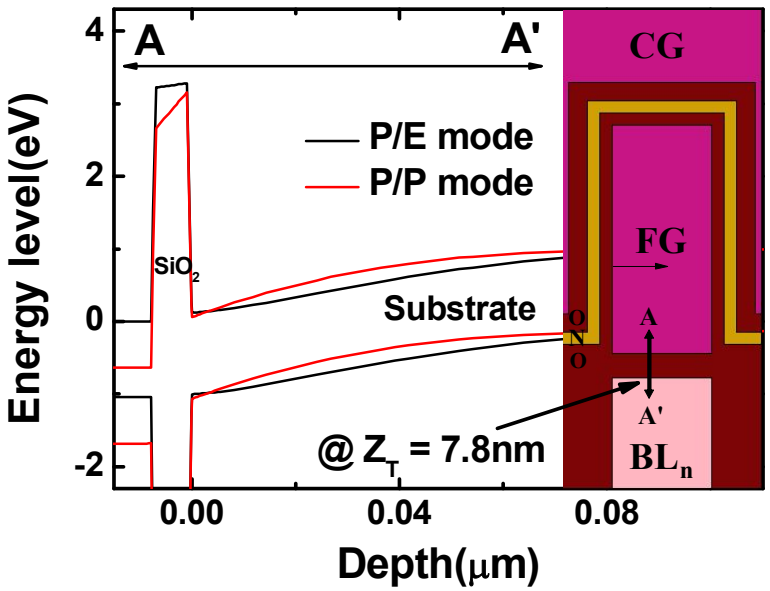


Fig. 8. Energy band diagrams in P/E and P/P modes at a fixed I_{BL}=100 nA.

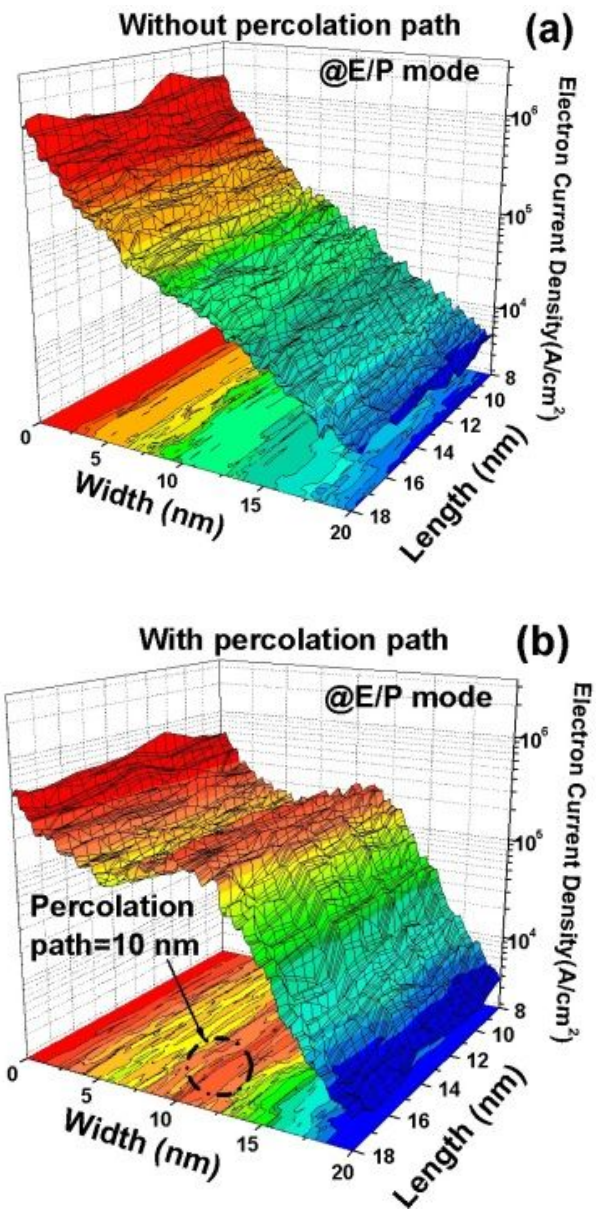


Fig. 9. (a) Electron current density without percolation path in E/P mode at I_{BL}=100 nA. (b) Electron current density with percolation path (10 nm) in E/P mode at I_{BL}=100 nA.

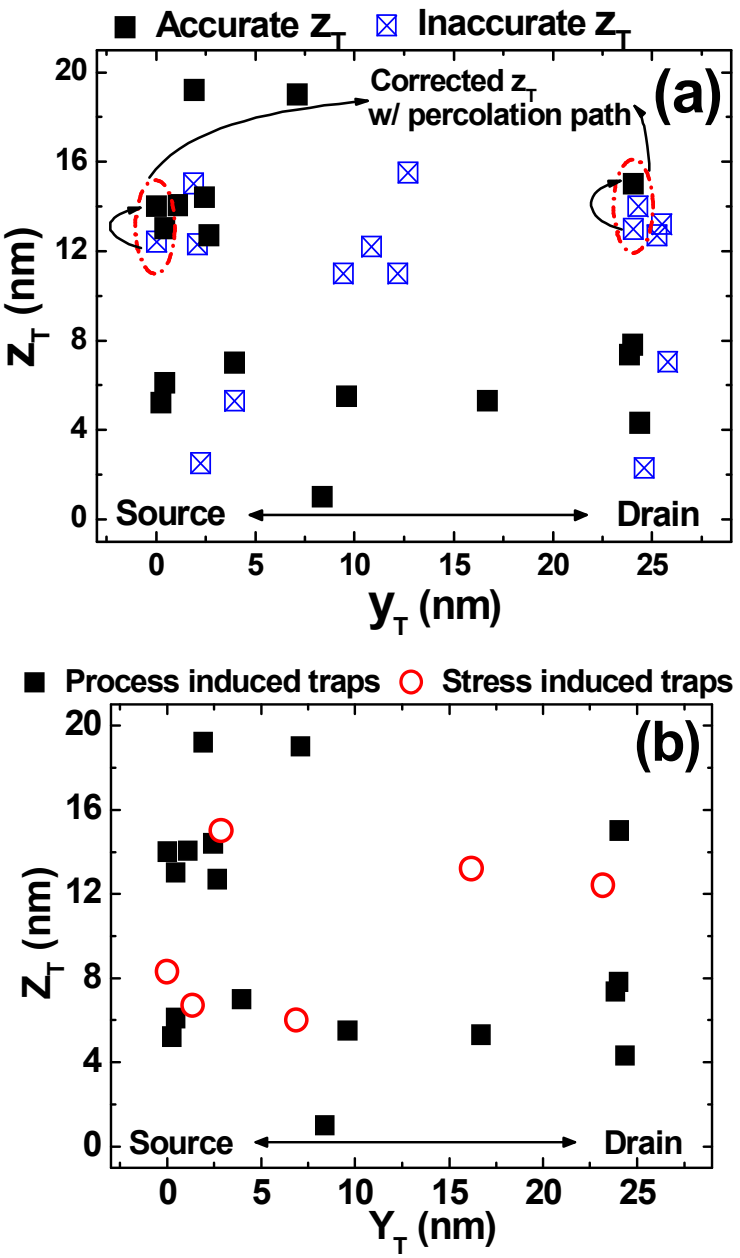


Fig. 10. Extracted trap position in z_T and y_T space of the tunneling oxide. (a) Crossed square symbols represent trap position with an error. Two trap positions are corrected by adopting percolation path. (b) The position of traps induced by process and cycling stress is compared.

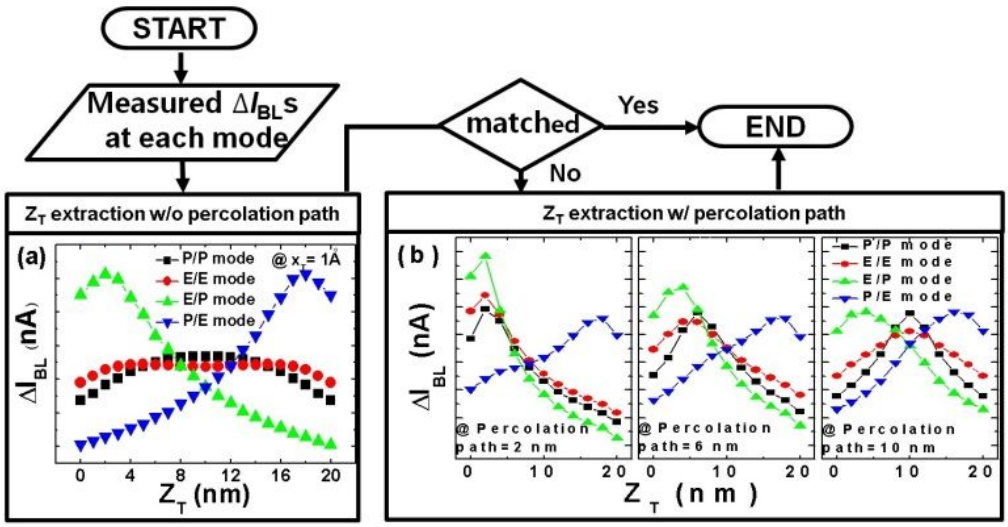


Fig. 11. Flow chart showing the process to extract z_T of traps without and with percolation path.

	P/P mode	E/E mode	E/P mode	P/E mode
τ_c (sec)	2.22×10^{-3}	5.46×10^{-3}	5.07×10^{-3}	3.64×10^{-3}
τ_e (sec)	9.03×10^{-3}	8.32×10^{-3}	8.46×10^{-3}	8.31×10^{-3}
τ (sec)	1.78×10^{-3}	3.29×10^{-3}	3.17×10^{-3}	2.53×10^{-3}
f_C (Hz)	89	48	50	62
ΔI_{BL}(nA)	67.3	57.2	63.5	45.9
$S_{I_{BL}} = \frac{4A\Delta I_{BL}{}^2\tau}{1+(2\pi f)^2\tau^2}$ $\tau = \frac{1}{\tau_c{}^{-1}+\tau_e{}^{-1}}$ $A = \frac{\tau}{(\tau_c+\tau_e)}$				

Table. 1 Extracted τ_c, τ_e, τ, f_c (corner frequency) and equations related to the extraction of τ and f_c

3. Characterization of RTN Generated by Process and Cycling Stress Induced Traps in 26 nm NAND Flash Memory

In this work, we characterized NAND flash cell strings fabricated with 26 nm technology. To check RTN generated by cycling stress induced trap, first, we measured I_{BL} in time domain and S_I/I_{BL}^2. Here, I_{BL} is 100 nA when V_{BL} and V_{PASS} are 0.8 and 6.5 V, respectively. Then we measured I_{BL} and S_I/I_{BL}^2 at the same bias condition after 1 k and 2 k cycling.

Fig. 12 (a) and (b) show I_{BL} of a cell before cycling and after 2000th cycling, respectively, in the time domain. Before the cycling stress, RTN was not observed. After 2000th cycling stress, RTN was generated and ΔI_{BL} was ~70 nA. In another cell as shown in Fig. 12 (c), we can observe small RTN before cycling, which means the trap was generated during fabrication process. In this figure, relatively fast and small RTN (ΔI_{BL} = 4.5 nA) is observed. After cycling the cell by 2000th, slow and large RTN (ΔI_{BL} = 40 nA) is generated in the cell as shown

in Fig. 12 (d).

Fig. 13 (a)- (d) show S_I/I_{BL}^2 corresponding to I_{BL} fluctuations of two different devices: (a)-(d) in Fig. 14, respectively. In Fig. 13 (a), S_I/I_{BL}^2 is increased significantly (more than several hundred times in the frequency range from 10 Hz to 2 kHz) by a cycling stress induced trap. Below 100 Hz, S_I/I_{BL}^2 after cycling is larger than that before cycling as shown in Fig. 13 (b). However, in the frequency range higher than 100 Hz, S_I/I_{BL}^2 of the device after cycling shows lower since the fresh device has a fast changing RTN with small amplitude.

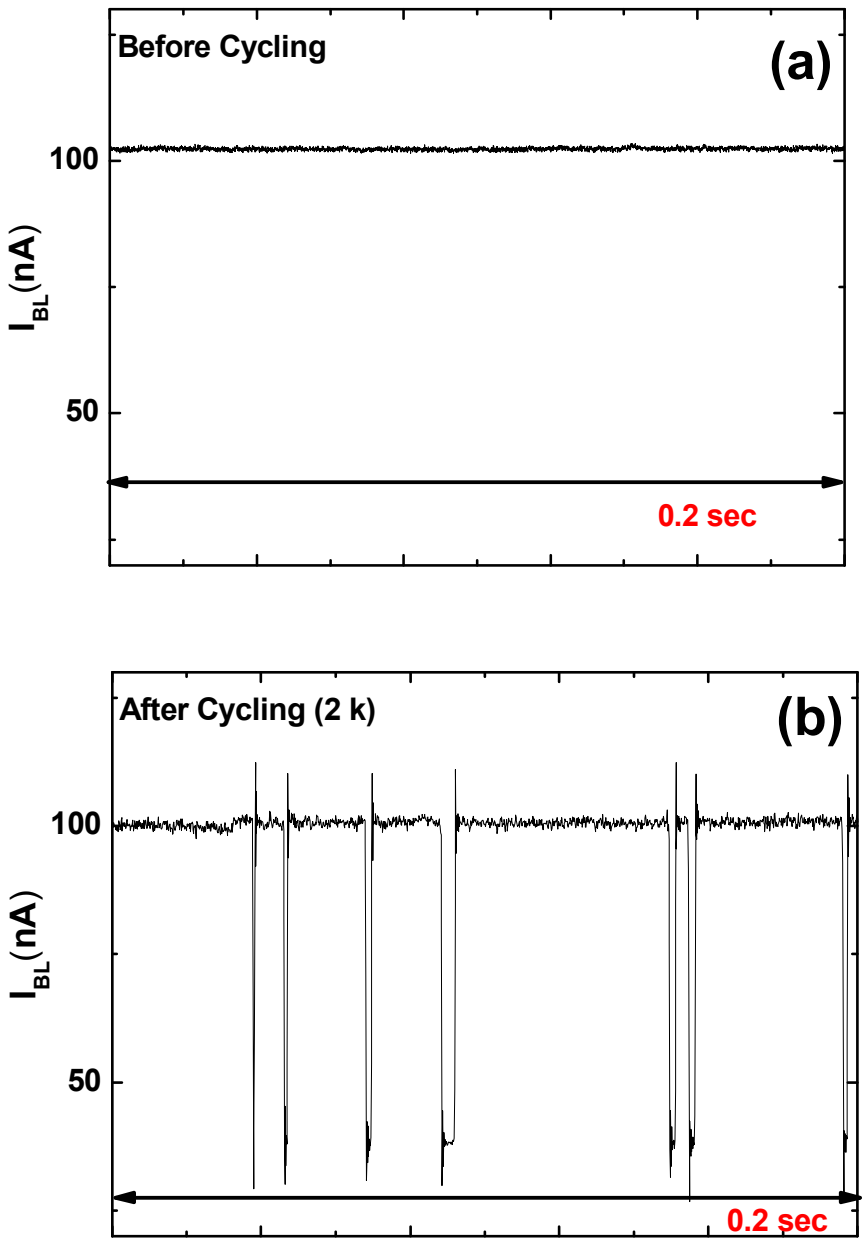
Then, Fig. 14 shows the 3-D position (x_T, y_T, and z_T) of extracted traps after cycling stress with the previous method. Big symbols represent the 3-D position of traps within the tunneling oxide. Small symbols stand for the trap position projected on y-z, x-z, and x-y planes. According to 7 traps extracted, the position of the traps generated by the cycling seems to be random in the tunneling oxide and need further research with more cells.

To analyze statistically the behavior of τ_c and τ_e with cycling, cumulative probability plots of τ_c, τ_e and $\ln(\tau_c/\tau_e)$ are shown in Fig. 15. These τ_c, τ_e are also

measured in the same condition as we did before (I_{BL} = 100 nA, V_{BL} = 0.8 V and V_{PASS} =6.5 V). Black-solid square represents process induced trap and red open dot represents stress induced trap. $\overline{\tau_c}$ and $\overline{\tau_e}$ of process induced trap are 7.6×10^{-3} and 2.1×10^{-2}, and stress induced trap are 6.1×10^{-3} and 2.5×10^{-3} which means average τ_c and τ_e of cycling stress induced RTN are about 2-3 times shorter compared to those of process induced RTN.

To understand the relationship between x_T and trap energy, we plot energy band diagram and extract the position of x_T at I_{BL} = 100 nA. In Fig. 5, we can observe extracted position of traps in terms of x_T and the energy. In the plot of E_{Cox}-E_T versus x_T under the flat band condition, averaged x_T of the stress induced traps is slightly closer to the channel. In the flat band condition, E_{Cox}-E_T decreases (upward on y-axis) with increasing x_T (to the left on x-axis). Under turn-on condition (I_{BL} = 100 nA), extracted E_{Cox}-E_Ts are nearly constant with increasing x_T by band bending as shown in the energy band diagram. By considering positive number (1.26 for process induced traps and 1.20 for cycling stress induced traps) of $\ln(\tau_c/\tau_e)$ shown in Fig. 16, the E_Ts of traps are located

generally at higher position than E_F in the energy band diagram.



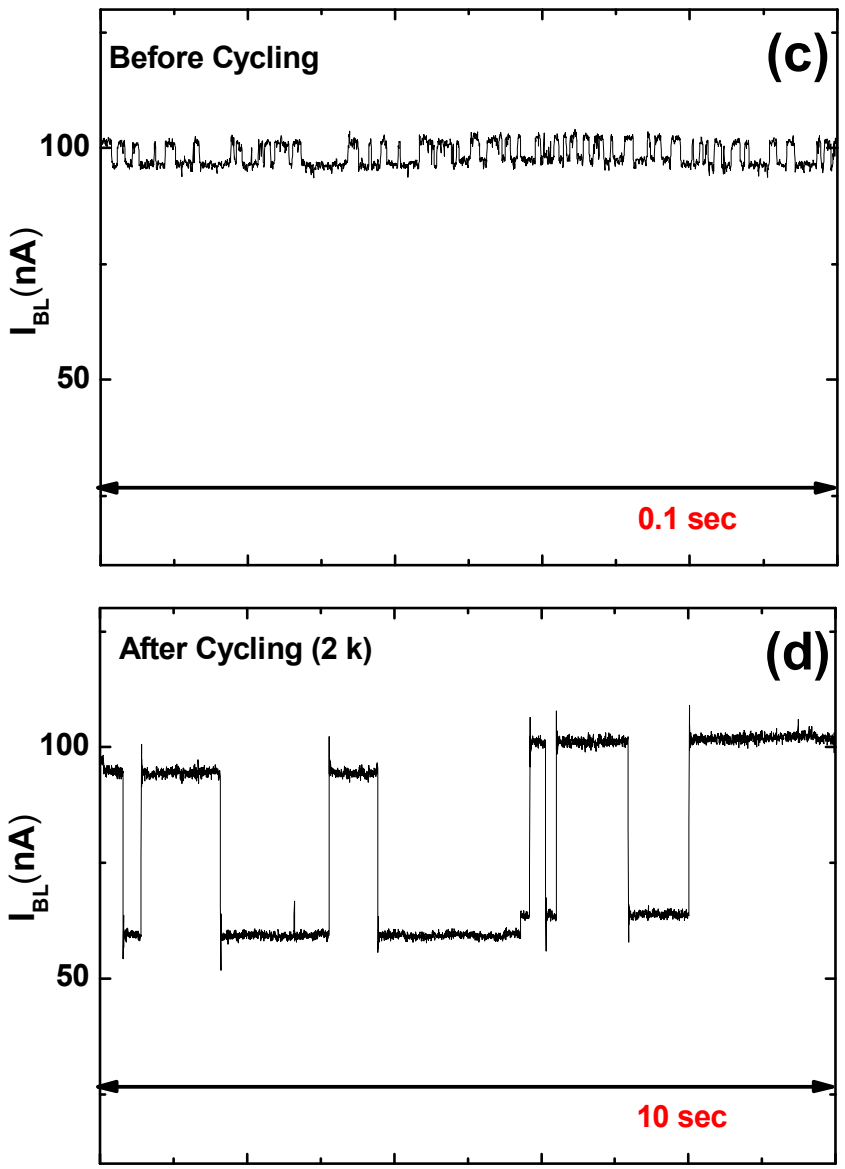


Fig. 12. Bit-line current fluctuation (ΔI_{BL}) in time domain before and after cycling stresses. (a)-(b) RTN is generated after 2k cycling. (c)-(d) Multi-level RTN is generated after 2k cycling.

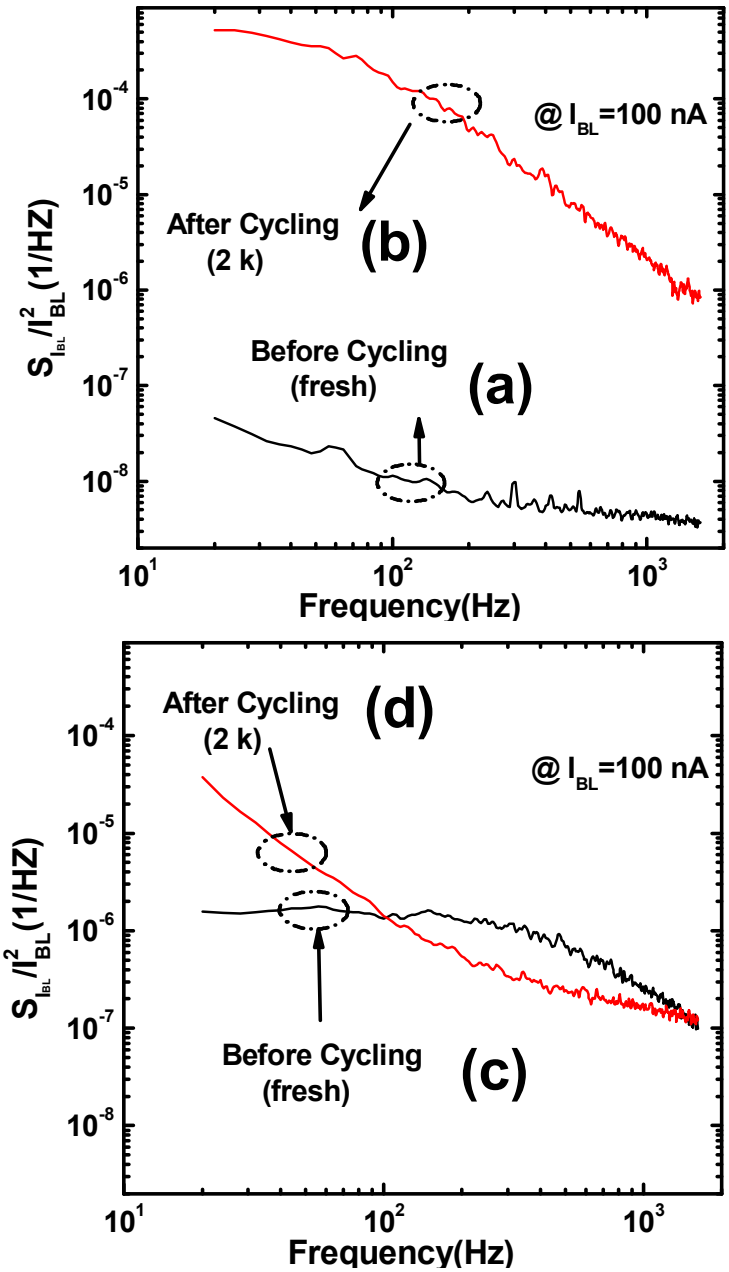


Fig. 13. Normalized noise power spectra corresponding to I_{BL} fluctuations in Fig. 14 (a)-(d)..

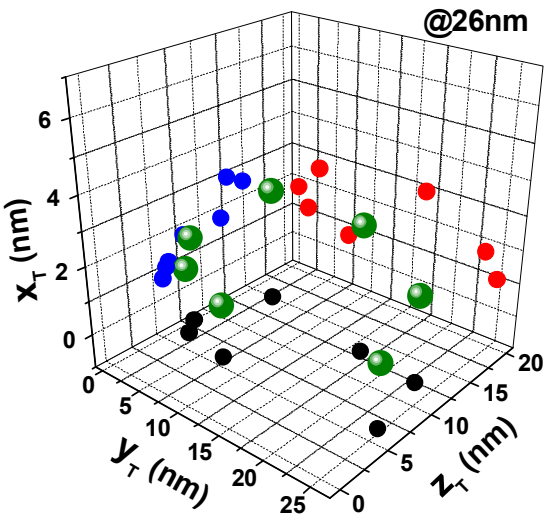


Fig. 14. Extracted x_T, y_T and z_T of cycling stress induced traps in the tunneling oxide. Small symbols are trap position projected on each plane.

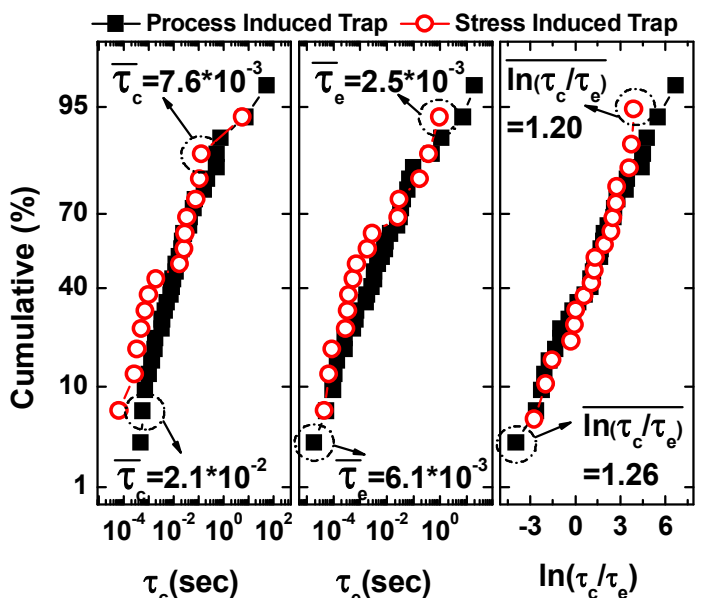


Fig. 15. Cumulative probability of τ_c, τ_e and $\ln(\tau_c/\tau_e)$ of process and cycling stress induced traps.

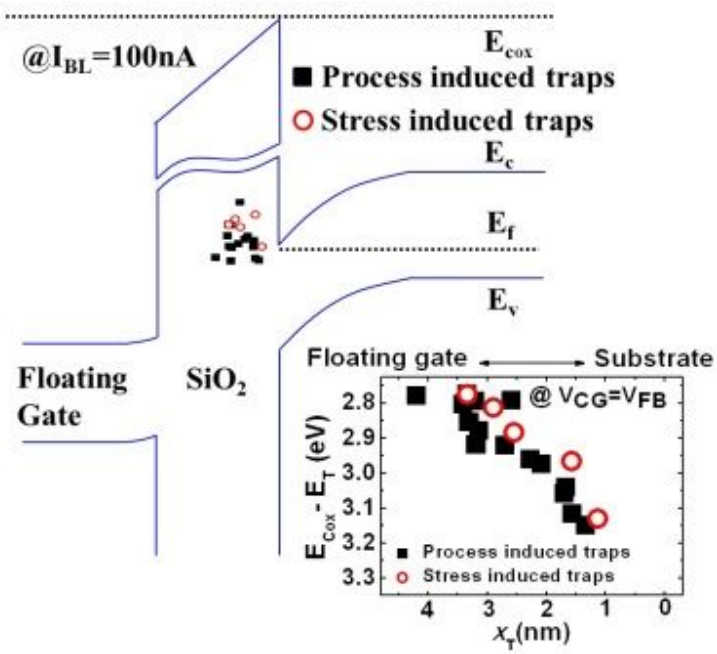


Fig. 16. Energy band diagram and extracted x_T position of traps at I_{BL}=100 nA.

5. Conclusion

In this paper, we have investigated key properties of RTNs from process and cycling stress induced traps through 3-D device simulation and measurement in 26 nm NAND flash memory. We investigated the effect of adjacent BL cell interference on low frequency noise in NAND flash memory cell strings. With states of adjacent cells, ΔI_{BL} and fc of Lorentzian spectrum were changed. Using measured current fluctuation ΔI_{BL} and extracted τ_c and τ_e with 4 modes, we calculated τ and f_c and extracted z_T. Through the z_T extracted, we drew the energy band diagrams in P/P and P/E modes. Then a new way based on percolation path was proposed to extract more accurate z_T position. Then, it was shown that read current fluctuation and noise power were increased significantly with cycling stress induced trap. 3-D trap position of stress induced traps was successfully extracted. The traps in the tunneling oxide generated during fabrication process were roughly located around both edges of the channel. Finally, we analyze the trap with the method charge pumping.

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초 록

최근, NAND 플래시 메모리는 저장매체로써 널리 쓰이고 있다. 이렇게 커지는 시장의 요구에 대응해서 초고집적도와 비트당 비용을 줄이고자 하는 요구가 증가하고 있다. 이러한 노력에 의해서 NAND Flash는 15 nm까지 사이즈 감소를 성공적으로 했다. 하지만 이러한 사이즈 감소로 인해서 NAND 플래시 메모리는 셀과 셀간의 간섭, 프로그램 포화현상 등 여러가지 문제에 직면하게 되었다. 이러한 문제들 가운데 특히 트랩에 전자가 들어갔다가 나왔다가 하는 현상으로 인한 Random Telegraph Noise(RTN)은 사이즈를 줄이려는 노력에 장애물이 되고 있다.

본 논문에서는 26나노 NAND 플래시 메모리(flash memory) 소자에 있어서 bit-line 전류 변동을 이용해서 터널링 산화물 안에 위치한 트랩의 3차원 위치와 트랩의 에너지가 분석되었다. 특히 주변 셀들의 상태를 이용해서 퍼컬레이션(percolation) 패스에 따라서 더욱 정확한

채널의 넓이 방향으로의 트랩위치(z_T)가 추출을 했다. 그리고 스트레스를 인가해서 트랩의 위치와 잡음 특성의 변화를 살펴보고, Charge pumping 방법을 사용해서 전반적인 잡음 특성을 확인할 수 있었다.

주요어: RTN, NAND 플래시 메모리, 트랩, Charge pumping, 열화, 스트레스

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